ECR #: 16
Title: A.G.P. to PCI Memory Write Support
Release Date: Feb. 10, 1997
Impact: Clarification
Spec Version: A.G.P. 1.0

Summary: Make A.G.P. to PCI Memory Write support optional.

Background: The current specification requires that PCI memory write transactions be supported where the master resides on either A.G.P. or PCI and has destination on the "other" bus segment (A.G.P. to PCI or PCI to A.G.P.). After evaluating the design complexity required to support this function a better understanding of the motivation to support this feature was initiated. The conclusion of the investigation was that support of memory write transactions from PCI to A.G.P. was required but transactions from A.G.P. to PCI was not. An application like Video Capture is an example where PCI to A.G.P. transfers are required for performance reasons. In this application the FrameBuffer is located on the A.G.P. bus while the capture device is added on the PCI bus segment. An application that required memory write transactions from A.G.P. to PCI was not found. If one is found in the future data can be copied into main memory and then either pushed by the host to the PCI target or if the PCI target can bus master it can fetch the data itself. This option may have a performance impact on the system due to consuming 2x the data badnwidth moving data into and out of main memory.

Change Current Specification as shown:

Replace the Paragraph in Section 2.4 that is labeled Bus-to-bus traffic capability

Bus-to-bus traffic capability bus masters on either the A.G.P. or the PCI bus will routinely access system memory. However, it is possible to also address targets on the other bus or port, which effectively requires a PCI-to-PCI bridge in the integrated chipset. Pushing WRITES through this bridge is fairly simple, whereas pushing READS through requires a complete bridge implementation, and it is not clear this would ever be utilized. Therefore, this interface specification only requires support for memory WRITES between a master on the PCI bus and a target on the A.G.P. bus.[1] Support of any other transaction between the two interfaces is optional and in general, should not assumed to work.

[1] By way of example, this allows for a video stream generator (e.g., capture, decode, etc.) on PCI to WRITE to the graphics frame buffer on the A.G.P.